Docket No.: 394-1597

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Seiji SAWADA et al. :

Serial No. 08/246,582 : Group Art Unit: 2511

Filed: May 19, 1994 : Examiner: A. Zarabian

For: TEST CIRCUIT IN CLOCK SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE

10/B
8-28-95

AMENDMENT

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

Sir:

The following amendment and remarks are submitted in response to the Official Action mailed June 8, 1995.

IN THE CLAIMS

Please amend claims 2, 4, 5 and 9 as follows.

2. (Twice Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of data output terminals;

a plurality of read means provided corresponding to said plurality of data output terminals for simultaneously reading data

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